Design of a Payload Avionics Interface Board for the VISORS (VIrtual SuperOptics with Reconfigurable Swarms) CubeSat Mission

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ABSTRACT

The following paper details the current state of the Payload Avionics Interface Board (PAIB) design for the VISORS mission. It is also intended as a resource for the students who will continue to develop its design into the future and manufacture the first realizations of this design. Context is provided for the entire VISORS mission as well as the need for this specific subsystem and how it contributes to success of the mission. The motivation and requirements for the PAIB are summarized to define the scope of the subsystem. Electrical and mechanical interfaces for the PAIB are discussed. Detail is provided for design decisions and component selection which has been completed thus far, with some guidance provided to aid in additional component selection. Finally, open action items and risks are discussed to set the stage for the next actions which must be completed to ensure development remains on schedule.

VISORS MISSION OVERVIEW

The VISORS (VIrtual SuperOptics with Reconfigurable Swarms) mission is an NSF funded CubeSat project initiated from the CubeSat Ideas Lab in February 2019. The goals of the project are to: 1) further knowledge of the solar corona and the heating processes that occur there, 2) conduct a technology demonstration of precise formation flying and intersatellite link technologies, and 3) to promote education and cross-pollination of CubeSat design knowledge between participating institutions.

These objectives are to be fulfilled with a distributed telescope system involving two 6U CubeSats. The Detector Spacecraft (DSC) and Optics Spacecraft (OSC) will align in LEO (Low-Earth Orbit) to take high resolution observations of the solar corona. The VISORS team is comprised of faculty and students from 9 education institutions, as well as engineers from the Laboratory for Atmospheric and Space Physics and NASA Goddard Space Flight Center. Blue Canyon Technologies is also contracted to produce the two spacecraft busses, allowing the rest of the team to focus on maturing the payload. Georgia Tech's role in this project is to serve as the Systems Engineering team and produce the cold gas propulsion system. As a major focus of the Systems Engineering team is to define the mechanical and electrical interfaces at the spacecraft level, the Georgia Tech team is developing the Payload Avionics Interface Board (PAIB) to facilitate the electrical interface between the spacecraft bus and various payload subsystems.

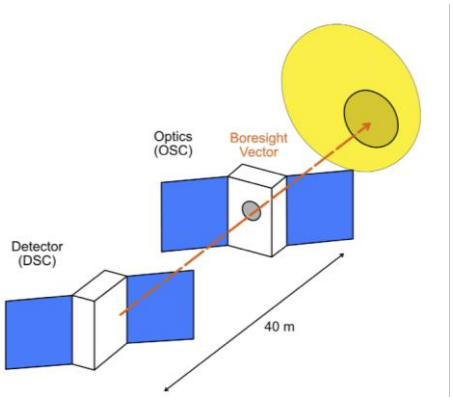

Figure 1: VISORS Formation Configuration [1]

Science Objectives

The minimum success science goal of the VISORS mission is to obtain a single image of the Sun in the He II 304 line with a resolution of 0.2 arcseconds, the current state of the art. To achieve these high-resolution images of this region in the solar corona an Extreme Ultraviolet (EUV) telescope is required as this is wavelength of light emitted in large quantities by the ionized Helium in the corona. The use of an EUV detector necessitates a 40-meter focal length, which cannot be achieved with conventional mirror-based optics as they struggle to meet the required diffraction limit, resulting in blurry images. As such the two-spacecraft formation is ideal – a single spacecraft with comparable performance would require a chassis more than twice the length of the James Webb Space

Telescope. Instead, off-axis photon sieve optics are employed to focus the EUV light onto the detector.

If the minimum success science objective is achieved, there are several extended objectives which the team is pursuing. First, the science team is looking to fully utilize the capabilities of the instrument to carry out observations with 0.12 arcseconds resolution to better observe theorized coronal filaments. This would result in the highest resolution images of the sun in EUV yet. The team also plans extended operations to observe the evolution of active regions of the sun over time at high resolution when the opportunities arise over the course of the mission. Due to the relatively low probability of a single successful image, data is collected in "science campaigns" where each science campaign is comprised of 10 science observations, each occurring over a single orbit. During a science observation, images are taken over a 10 second period at a rate of 2.-7.5 frames per second. This results in up to 75 images per science observation. With successful extended objectives, the VISORS mission is poised to shed new light into the heating processes occurring in the solar corona.

Engineering Objectives

In addition to the ambitious science objectives of the VISORS mission there are several untested technologies which will by flying for the first time. Because of the unique challenges which arise to fulfill the mission objectives, these experimental systems are required for mission success. This allows the VISORS mission to serve as a proof-of-concept opportunity for these systems, providing an opportunity to fast-track these technologies to TRL 7 and potential use on future missions. These systems are the GNC (Guidance, Navigation, and Control) software and the ISL (Inter-Satellite Link) system. Note that a mission specific propulsion system will also be flown with flight heritage as well as the one-off PAIB.

For an in focus, on target, and unsmeared image to be collected, stringent relative and inertial maneuvering and pointing is essential. The GNC software employs filtering algorithms using GPS data to resolve the relative positions of the spacecraft. These algorithms must achieve less than 18 mm lateral position error, 15 mm longitudinal error, and 200 micrometers per second of lateral velocity error. This is achieved using the DiGiTal (Distributed Multi-GNSS Timing and Localization for nanosatellites) algorithm/filter [2]. The choice of a near-polar orbit allows for passive safety for two orbits during science operations and multiple days during standby operations. This provides the confidence needed to conduct the science proximity operations.

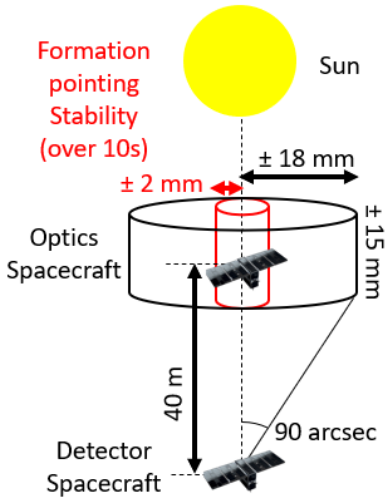

Figure 2: VISORS GNC Observation Requirements [3]

To allow for this relative navigation algorithm to resolve the state of both spacecraft, an ISL system is required to allow for GNSS data to be shared across the two spacecraft. This system is called XLINK on the VISORS mission and operates at 5.8 GHz. This allows for a wide bandwidth to be utilized when the spacecraft are within 1 km of one another for high data rates, which can be throttled down at longer ranges for a more robust link. This system employs patch antennas on each face of the spacecraft, resulting in a near omnidirectional link. As the spacecraft slew relative to one another, the XLINK system can cycle between pairs of antennas to maintain the link. The system is built around a COTS (commercial-off-the-shelf) SDR (software defined radio) supplemented with additional functionality to achieve its requirements.

Detector Spacecraft Design

The DSC and OSC are both built from a COTS BCT bus, known as the XB1 [4]. This bus provides the 6U chassis to house the subsystems onboard the spacecraft and will be delivered to Georgia Tech with its avionics box already installed. This avionics box contains all the fundamental subsystems required for a functional spacecraft. The onboard EPS (Electrical Power System) includes the necessary solar cells (mounted on external deployables), power regulators and battery chargers, battery cells, and output voltage regulators. 3.3 V, 5 V, and unregulated power supplies are provided by the bus. The C&DH (Command and Data Handling) subsystem includes a Xilinx FPGA (Field Programmable Gate Array), ADC (Analog to Digital Converter), onboard volatile and non-volatile memory, and serial line drivers. The available serial lines include a Spacewire interface, two RS-422 interfaces, and a SPI interface. The ADCS (Attitude Determination and

Control System) is made up of a star tracker and IMU (Inertial Measurement Unit) for attitude resolution and a L1/L2 GPS antenna and receiver for position data. Attitude is controlled using three reaction wheels paired with three torque rods for angular momentum desaturation. The DSC has an additional star tracker in the payload section to increase the attitude resolution of the DSC. Finally, the COM (communications) subsystem is comprised of a downlink telemetry memory buffer, UHF (Ultra-High Frequency) TT&C (Telemetry, Tracking, and Command) radio system, and a monopole whip antenna deployable. The GNC algorithm is stored in an HSA (Hosted Software Application) within the BCT bus along with the payload CSM (Central State Machine) and GNC to Prop Converter. This converter transforms delta V vector outputs received from the GNC algorithm into discrete valve firings which are sent to the propulsion system.

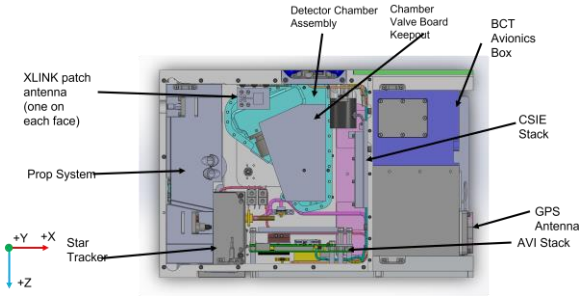

Figure 3: VISORS DSC Internal View

The propulsion system is a cold gas design utilizing R-236fa non-toxic refrigerant for propellant. The tanks and structure of the system are 3D printed using SOMOS PerFORM. The system architecture and control board are derived from previous designs manufactured and flown by GT. The control board communicates with the BCT bus over an RS-422 interface. The nozzle impulse vectors are not coincident with the spacecraft center of mass, so reaction wheels must counteract the resultant moment, which somewhat limits the frequency and magnitude of propulsive maneuvers. The propulsion system on the DSC and OSC are functionally identical with identical control boards, but the OSC has a larger tank allowing for that spacecraft to provide almost two thirds of the total deltaV for both spacecraft.

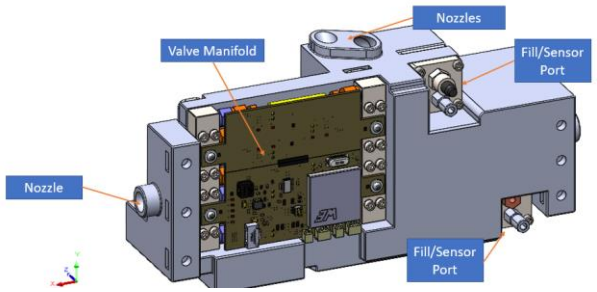

Figure 4: VISORS Propulsion System [5]

The Avionics Stack is made up of several XLINK boards as well as the PAIB. The PAIB sits on the bottom-most part of the stack, closest to the bus chassis wall. The PAIB interfaces with the BCT bus over an RS-422 line. Mounted above the PAIB is the XLINK SDR as well as an L-Shaped Amplifier board. The electronics boards interface with the PAIB through a series of mezzanine (also called board-to-board) connectors, through which communication to the bus is achieved over SPI. The amplifier boards significantly improve the performance of the SDR, increasing the link range from under 1 km to over 10 km. Above the SDR and amplifiers is the Switching Board, which contains the switches needed to alternate between transmitting antennas, as well as circulators, which allow each antenna to operate half-duplex despite individual TX and RX channels on the SDR. The XLINK patch antennas are built into PCB's (printed circuit boards), with one on each face of the spacecraft pointing outwards.

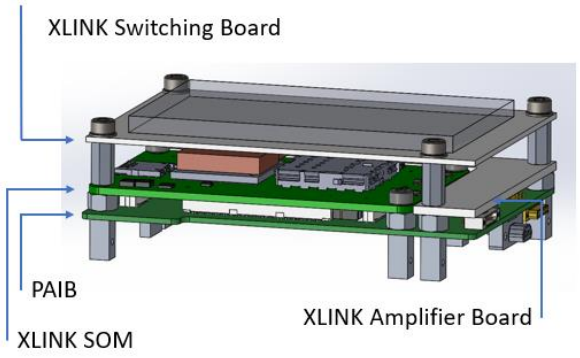

Figure 5: VISORS Avionics Stack

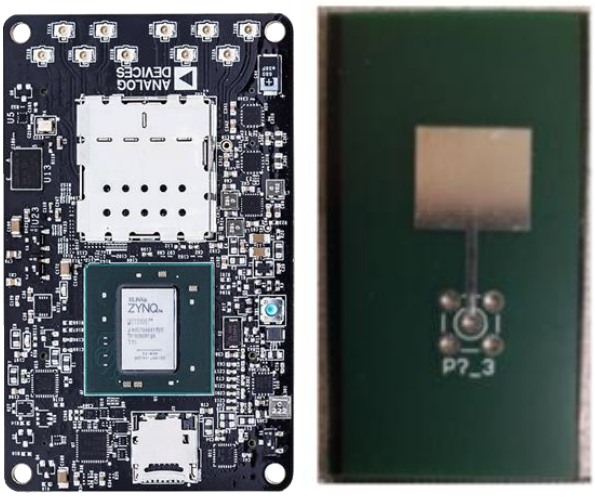

Figure 6: VISORS XLINK SDR and Antenna [6]

The DIA (Detector Instrument Assembly) is comprised of the detector chamber, door mechanism, image processing electronics, and support electronics. The detector chamber is made of aluminum and contains the required optics (apart from the photon sieve on the OSC). The Detector Chamber contains a filter to isolate the EUV light as it enters the detector, a mirror to redirect the light onto the detector chip (assisting in maintaining the small detector form factor), and the Detector Chamber Board. The Detector Chamber Board support the CMOS detector chip. The detector door is a one-shot NEA (non-explosive actuator) mechanism opened using a torsion spring which is hermetically sealed to contain the dry nitrogen inside the detector chamber, protecting the optics during I&T (Integration and Test) and launch. The CSIE (Compact Spectral Imaging Electronics) is comprised of a two-board stack which is located outside the detector chamber and performs lossy and lossless compression of images. The CSIE communicates with the BCT bus over a Spacewire interface & SE (single-ended) digital interface, and to the PAIB over a much slower RS-422 interface. Finally, the CVB (Chamber Valve Board) contains electronics to monitor and control the pressure of the dry nitrogen in the detector chamber during commissioning. It is comprised of a solenoid valve which vents the dry nitrogen and monitors the pressure in the chamber with a PT (pressure transducer). The CVB communicates with the PAIB over an I2C interface (for the PT) and SE digital interface (for the solenoid).

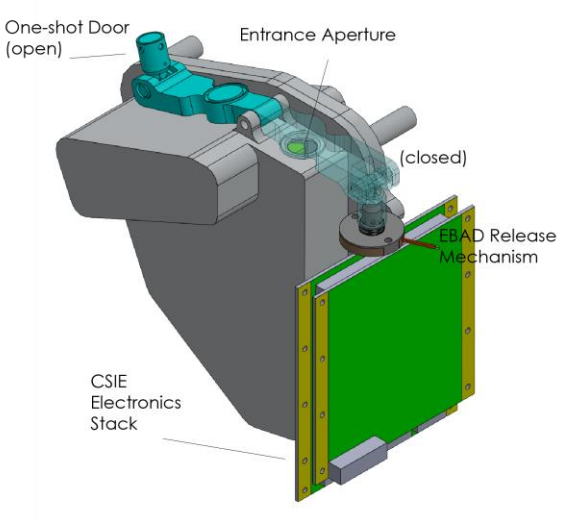

Figure 7: VISORS DIA (CVB not pictured) [7]

Optics Spacecraft Design

The OSC is comprised of an identical chassis and XB1 avionics box provided by BCT, as well as avionics stack and a functionally identical propulsion unit. However, the OSC does not contain any of the DIA systems, which are replaced by the photon sieve and LRF (Laser Rangefinder).

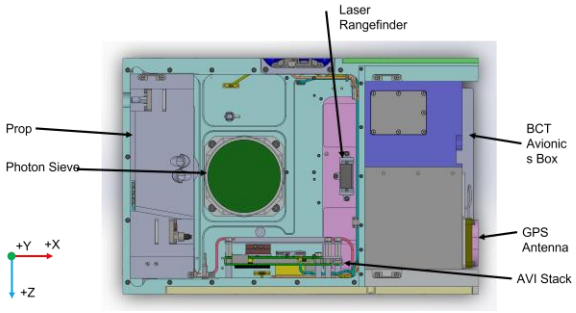

Figure 8: VISORS OSC Internal View

The photon sieve is a type of diffraction optics used to focus light. It is similar to a Fresnel zone plate but employs pinholes instead of concentric rings for diffraction. This photon sieve is made of a thin sheet of silicon, mounted in an aluminum structure. The photon sieve used on VISORS is unique in that it is asymmetrical, so the focal center of the sieve is not the geometric center and is actually not contained within the sieve at all. As such the sieve is mounted away from the center of mass of the OSC, so that the optical center is near the spacecraft's center of mass. The photon sieve is a passive instrument and requires no electrical interface.

Figure 9: VISORS Photon Sieve Prototype [8]

The second unique subsystem aboard the OSC is the LRF. The LRF is a low-cost consumer part whose ranging data between the OSC and DSC is used to supplement the GPS data for determining the quality of images prior to downlink. It is not required for mission success and is intended just to provide additional support telemetry for images. The LRF is potted into a mount using epoxy and bolted to the OSC chassis pointing outward and towards the DSC during observations. The DSC has a surface plated in white thermal control paint to provide a reflective target for the LRF. The LRF communicates with the PAIB utilizing LVTTL (Low Voltage Transistor to Transistor Logic) at 3.3-volt logic levels.

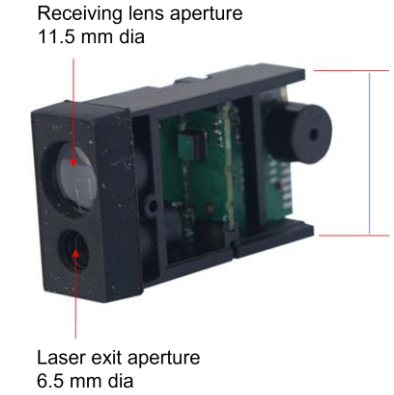

Figure 10: VISORS Laser Rangefinder [9]

PAYLOAD AVIONICS INTERFACE BOARD OVERVIEW

The VISORS architecture of utilizing a COTS bus alongside several custom subsystems built by multiple institutions results in a more complex interface challenge than spacecraft where design and production is centrally located to one or a few groups. In addition, the BCT bus interfaces are being closed out while subsystems are still developing their technology, making interface requirement flow down a challenge, with the torch being burnt from both ends. As GT is serving as the system integrator and Systems Engineering team, an additional subsystem is required to facilitate the electrical interfaces between the bus and payload subsystems.

Motivation

The PAIB serves to resolve these integration challenges with a single PCB (printed circuit board). There are three major functions the PAIB serves to allow the VISORS mission to successfully complete its objective.

First, the PAIB must break out the BCT power rails (3.3V, 5V, and unregulated) to each subsystem. The PAIB has individual load switching for each subsystem as well as current monitoring for these subsystems. As multiple payload subsystems utilize the same power rails, directly connecting the BCT bus to these subsystems would require all systems utilizing the same voltage level to turn on and off together. This limits operation and effectively forces all subsystems to be on through the duration of the mission, drawing unnecessary power. Similarly, the additional current monitoring allows for each subsystem's power draw to be carefully observed, as opposed to an entire voltage rail. This also allows for individual subsystems to be power cycled if an over-current event occurs and makes such events more easily detectable. Voltage monitoring is not employed on the PAIB as this functionality is included on the BCT bus and is identical over all payload subsystems using the same voltage level.

Next, the PAIB provides electrical and data passthroughs between the BCT bus and payload subsystems. The BCT interface splits power and data lines over three distinct connectors and are only roughly grouped by subsystem. The alternative approach would be complex and volume dense harnessing assemblies with several connectors and would result in complex cable runs. Instead, the PAIB accepts these three BCT electrical interfaces and breaks them out to a single connector for each subsystem using traces on the board. This simplifies the interfaces as well as the routing required. The PAIB also supplements the limited serial interface options available on the BCT bus to interface with the CVB over I2C and the LRF over LVTTL. The data from these subsystems is grouped into telemetry packets and sent over its RS-422 interface with the BCT bus.

The final function the PAIB provides the VISORS mission is supplemental non-volatile flash memory for image data. Due to the slow image downlink rates as the TT&C UHF can only transmit to 19.2 kbps (where a single raw image is 48 Mb), the mission ConOps requires all images from the lifetime of the mission to be saved onboard the spacecraft. This approach allows for GNC telemetry and low-resolution image

thumbnails to be downlinked first, and the larger images to be sent when downlink time is available. However, the BCT bus only has 3.25 GB memory available for images, which can only save approximately half a science campaign of data, making this approach unsustainable. As such an RS-422 interface is implemented between the CSIE and PAIB to allow for the images to be backed up on the PAIB. The PAIB is designed to have sufficient non-volatile memory to save every full resolution image recorded over the lifetime of the mission.

Development Timeline

As of the writing of this report the VISORS project CDR (critical design review) has been completed and the PAIB mechanical and electrical interfaces have been fully defined. The PAIB functional design has been completed resulting in selection of critical components. The next steps are to design the board schematic as well as specify remaining support components (resistors, capacitors, inductors, oscillators, etc.). The spring of 2022 will be utilized for this effort, along with designing the first EDUs (engineering development units) as well as writing the FSW (flight software). The diagram below outlines the overarching development schedule. It is critical to the project level schedule to deliver functional EDUs at the end of March 2022, and no later than April 2022.

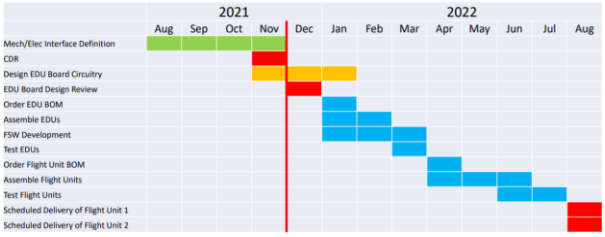

Figure 11: PAIB High Level Schedule

#	Task	Days Needed
1	Level 1 Reqs Identified	2
2	Level 2 Reqs Identified	2
3	GSE Identified	2
4	Final FBD Delivered	7
5	Final BOM	7
6	EPS Circuitry Designed	14
7	C&DH Circuitry Designed	14
8	EDU Board Designed	7
9	EDU Board Review	1
10	EDU Breakout Board Designed	7
11	EDU Board Parts Purchased	1
12	LEAD TIME	14
13	EDU Board Assembled	7
14	EDU Breakout Board Assembled	2
15	EDU Cold Testing	1
16	EDU Hot Testing	2
17	Software Development	60
18	Software Testing and Debugging	30
19	SW Board Functional Test Developed	14

#	Task	Days Needed
20	Integrated System Testing of Board	14
21	Staking and Conformal Coating	2
22	EDU Vibe Testing	7
23	EDU TVAC Testing	7
24	LEAD TIME	14
25	FM-1/-2 Board Parts Purchased	1
26	FM-1 Board Assembled	7
27	FM-1 Cold Testing	1
28	FM-1 Hot Testing	2
29	FM-1 Staking and Conformal Coating	2
30	FM-2 Board Assembled	7
31	FM-2 Cold Testing	1
32	FM-2 Hot Testing	2
33	FM-2 Staking and Conformal Coating	2
34	FM Vibe Testing	7
35	FM TVAC Testing	7
36	FM Checkout Testing and Char	14
37	First FM Delivered	7
38	Second FM Delivered	7

Figure 12: PAIB Detailed Task List

PAIB REQUIREMENTS

There are several functional and interface requirements levied on the PAIB to ensure it preforms as needed by the VISORS system, on both spacecraft. Note that not all requirements are listed here, and some requirements are obsolete or are under modification at the time this report was written. Always refer to the mission RVCM (requirements verification matrix) in the project documentation for current requirements.

Functional Requirements

1. *AVI-002: "The payload portion of each spacecraft bus shall contain hardware that serves as the power conditioning and distribution for the payload subsystems."* This requirement ensures the PAIB provides power to the payload subsystems, monitors the power draw of each payload, and has the capability to autonomously shut down in the case of an overcurrent event. These functionalities are not available on the BCT bus.

2. *AVI-004 through AVI-006:* Details the need to route communication between the XLINK, propulsion, CVB, LRF, and CSIE instruments to the BCT bus, and by extension to the GNC HSA. The PAIB does not process any of this data but rather simply routes these signals from connector to connector.

3. *AVI-007: "On the detector spacecraft, the avionics board shall receive and store images from the detector assembly."* This addresses the need to store all images collected over the lifetime of the VISORS mission to the PAIB for later downlink.

4. *AVI-013: "On the detector spacecraft, the avionics board shall have non-volatile memory of no less than 32 GB."* Such a requirement ensures there is sufficient non-volatile memory available for images over the mission lifetime.

5. *AVI-016: "The avionics board shall be capable of handling a minimum data rate of 115.2 kbps from the bus flight computer."* This data rate is the planned RS-422 speed between the PAIB and BCT bus and is constrained by the capabilities of the BCT bus.

6. *AVI-019: "The avionics board shall be designed to withstand the total ionizing dose over the mission life in the specified orbit of [TBD]."* While this requirement is still TBD, the electronics on the PAIB should be resistant up to 10 krad of TID (total ionizing dose), taking the shielding effects of the aluminum chassis into account. Radiation analysis should be conducted to determine on-orbit expected TID for the mission lifetime and extended operations.

Interface Requirements

1. *AVI-020: "The avionics board shall have a mechanical interface with the bus chassis for attachment as defined in the PAIB ICD."* The interface as defined in the PAIB ICD is the interface design BCT is utilizing for mounting the PAIB (and by extension rest of the avionics stack). It would be difficult to deviate from this design due to maturity of BCT bus mechanical design.

2. *AVI-021: "The avionics board shall have an electrical interface for data and power transmission with the bus avionics unit as defined in the VISORS XB1 Flight Unit ICD."* The interface with the BCT bus was determined based on payload needs and capabilities of the COTS XB1, and the electrical interface design is also far in the design process at BCT.

3. *AVI-022: "The avionics board shall have an electrical interface for data and power transmission with the propulsion system as defined in the VISORS Propulsion ICD."* The PAIB is more flexible in its design versus the propulsion system due to the heritage of the propulsion controller board. As such the interface flows from the PROP ICD. The following requirements are defined in the same vein

4. *AVI-023: "The avionics board shall have an electrical interface for data and power transmission with the ISL hardware as defined in the XLINK ICD (TBR)."*

5. *AVI-024: "On the detector spacecraft, the avionics board shall have an electrical interface for data and power with the detector assembly as defined in the CSIE ICD and the Chamber Valve Board ICD (TBR)."*

PAIB SYSTEM ARCHITECTURE

Technical Specifications

The baseline/current design of the PAIB has the following specifications:

1. Operating Voltage: 3.3 V
2. Peak Power Consumption: 857 mW
3. Idle Power Consumption: 60 mW
4. Operating Temperatures: -40 to 85 C
5. Survival Temperatures: -40 to 125 C
6. Mass: 105 grams (expected to increase ~10%)
7. Volumetric Envelope: 4.90" x 3.35" x 0.50"
8. Cost per Unit (Current Best Estimate): $4,250

Mechanical Interface

The PAIB is constrained to the Avionics Stack with 7-M4 clearance holes. M4 standoffs are bolted through these mounting holes to fasten the PAIB to the other boards in the avionics stack (SDR, amplifier, switching), as well as to the adapter standoffs. These adapter standoffs (female to female) accept M4 threaded standoffs on one side, and 4-40 socket head screws on the other. The socket head machine screws connect the Avionics Stack to the bus chassis using counterbored through holes from the exterior (+Z face of chassis). The interface for the PAIB is identical on the OSC and DSC, as is its location. The drawing below provides additional detail of the mechanical interfaces and envelope and is provided in detail in the PAIB ICD

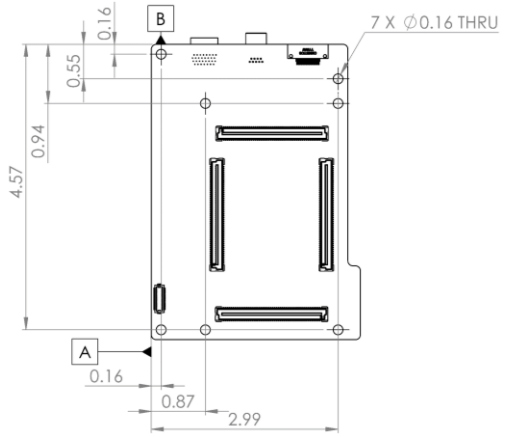

Figure 13: PAIB Mechanical Interfaces (inches)

Power Interfaces

As mentioned previously the power interface of the PAIB is driven by the BCT bus and payload subsystem designs. The BCT bus directs the energy of the battery into six independent load switches [4]. These load switches can be turned on or off individually autonomously if the bus transitions modes or in response to a ground command. Each load switch has an associated voltage level and max allowable current draw. The voltage level of the 3.3 V and 5 V load switches are controlled by switching buck converters which condition down the bus battery voltage. The 8.7-12.6 V unregulated line is connected directly to the batteries and will supply a voltage dependent on the SOC (state-of-charge) of the battery itself. Each load switch also has in-line voltage and current monitoring, which is downlinked alongside the other bus telemetry. Note that the BCT bus has additional load switches beyond those listed which are used to power BCT internal components. The BCT load switches connect to the payload subsystems as shown in Table 1.

Table 1: BCT Load Switches

Load Switch	Voltage Level	Current Limit
LD4 and LD6*	Bus Unregulated	3 A
LD11	Bus Unregulated	1 A
LD2**	5 V	1.5 A
LD5**	5 V	1.5 A
LD10	3.3 V	1 A

* These two load switches are tied in parallel at the bus output.

**LD2 and LD5 should not be tied together on the spacecraft due to differing voltage sources/references

These load switch sources are broken out to the individual subsystems. The voltages required and expected max currents for each payload subsystem are detailed in Table 2.

Table 2: Payload Subsystem Power Draws

Payload	Voltage Level	Max Expected Current
CVB (DSC only)	Bus Unregulated	2 A
	3.3 V	0.012 A
CSIE (DSC only)	5 V	1.552 A
PROP	Bus Unregulated	2.834 A
	5 V	0.054 A
XLINK Amp	5 V	0.751 A
XLINK SDR	5 V	1 A
PAIB	3.3 V	0.260 A
LRF (OSC only)	3.3 V	0.3 A

The maximum expected current of the CVB is driven by the one-shot solenoid valve and the max expected current of the CSIE is driven by the one-shot NEA door mechanism. These events will occur during the commissioning phase of the spacecraft and will not occur in parallel with each other or propulsion system actuations. The current draw of the CSIE for the remainder of the mission when it is active (during observations or data transfer) is less than 1 amp.

The intended mission ConOps results in a peak power condition for both the OSC and DSC. It is critical to ensure no current limits imposed by the BCT bus are violated during these conditions or damage to the bus is possible. The DSC and OSC max power conditions are given in Table 3 and Table 4.

Table 3: DSC Maximum Power Condition

Voltage Rail	Bus Max Allowable Current	Max Expected Current	Safety Margin
3.3 V	1000 mA	272 mA	72.8%
5 V [A]*	1500 mA	775 mA	48.4%
5 V [B]*	1500 mA	1000 mA	33.3%
Unregulated	4000 mA	2834 mA	29.1%

Table 4: OSC Maximum Power Condition

Voltage Rail	Bus Max Allowable Current	Max Expected Current	Safety Margin
3.3 V	1000 mA	560 mA	44.0%
5 V [A]*	1500 mA	775 mA	48.4%
5 V [B]*	1500 mA	1000 mA	33.3%
Unregulated	4000 mA	2834 mA	29.1%

*5V [A] and 5V [B] should not be tied together on the spacecraft due to differing voltage sources/references

With a safety margin of just under 30%, the payload subsystems should not violate the current limits of the bus during nominal operations. In the case of an anomaly driving the current above these limits, protection circuitry onboard the PAIB will shut off the malfunctioning system.

The PAIB bus and payload power interfaces are detailed in Figure 14.

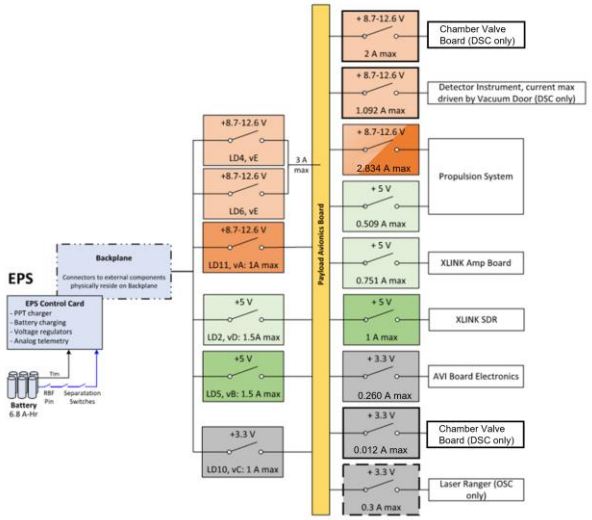

Figure 14: PAIB Power Interfaces Functional Diagram

Each payload subsystem has a dedicated power line with in-line load switches (with automatic overcurrent shutoff) as well as shunt resistors and current sense amplifier IC's (integrated circuits) for measuring current draw of each subsystem on the PAIB. Note these are distinct from the BCT bus load switches. Because of the single point of failure for each subsystem at this power interface, redundant load switches are utilized in parallel to provide single fault tolerance protection for the load switches. If one load switch has an unexpected failure (most likely from ionizing radiation) the redundant load switch can be used to switch power on and off for the subsystem. This only protects from open-circuit failures, however. If the load switches fail closed the parallel load switch will not be able to turn the subsystem off. This is deemed as acceptable as the typical failure mode of parts with a MOSFET (magnetic-oxide semiconductor field effector transistor) architecture is to fail open and single fault tolerance for both open and closed conditions would require 4-8 load switches per subsystem. If sufficient footprint is available on the PAIB it is suggested to implement this more complex architecture. If one of the current sensing IC's fails, it will result in a degraded understanding of the state of that respective subsystem but does not pose direct risk to the system. The automatic overcurrent shutoff of the PAIB load switches protects the shunt resistors and PCB traces from damage should a dead-short occur.

Data Interfaces

Similarly to the power interfaces, the data interfaces are driven by the requirements and design of the payload subsystems and capabilities of the COTS BCT bus. Unlike the power interfaces however, little additional hardware and software design is required to facilitate the interface between the BCT bus and payload subsystems, as all complex subsystems have a one-to-one serial communications interface with the BCT bus, so no multiplexing is required. The CVB and LRF communicate to the BCT bus through the PAIB processor and communications line, but the simplicity of these systems allow for their telemetry to be integrated into existing PAIB health packet generation and command architectures. The CSIE has a communications line with the PAIB processor to back up science images. Finally, the PAIB also serves as a digital signal passthrough for the XLINK system to route controls signals from the SDR to the amplifiers and switches. Table 5 details the data interfaces facilitated by the PAIB. Note that all data interfaces are half or full duplex, so communication is possible in both directions (from/to).

Table 5: PAIB Data Interfaces

Data Interface	Type	Data/Clock Rate
Bus from/to CSIE	Spacewire	25,000 kbps
Bus from/to PROP	RS-422	115.2 kbps
Bus from/to XLINK	SPI	2,000 kHz*
Bus from/to PAIB	RS-422	115.2 kbps
PAIB from/to CSIE	RS-422	921.6 kbps
PAIB from/to CVB	I2C	100 kHz*
PAIB from/to LRF	LVTTL	19.2 kbps
PAIB from/to XLINK	Digital Only	N/A

*Data rate and clock rate for synchronous communications are effectively equivalent but specified in Hz to distinguish from asynchronous communications.

The DSC and OSC have slightly different data interfaces due to the presence of the LRF on the OSC and the CVB onboard the DSC. Figure 15 and Figure 16 show the data infaces of each spacecraft. Note the XLINK control lines are omitted here for clarity as no data is leaving or entering the XLINK subsystem over that interface.

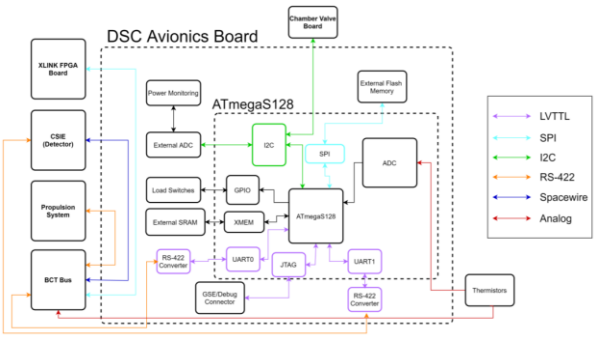

Figure 15: DSC Data Interfaces

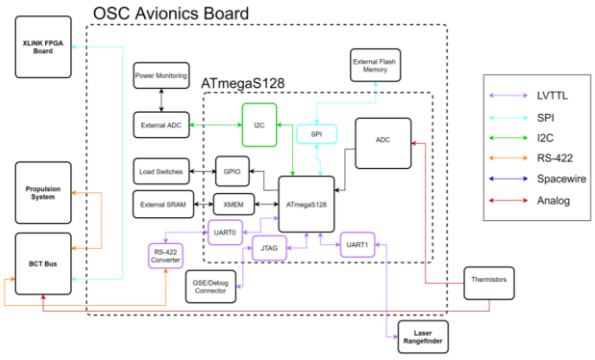

Figure 16: OSC Data Interfaces

The Bus-CSIE data interface implements Spacewire protocol [10]. Spacewire utilizes an 8-wire interface and is based off LVDS (Low Voltage Differential Signaling) interfaces, operating at +/- 1.2 V logic levels. Spacewire is an asynchronous serial interface and is full duplex (can receive and send data simultaneously). Differential signaling utilizes a twisted pair of wires which terminate at the destination with a 100-ohm resistor, meaning the voltage in one wire is effectively positive, while the other is negative to send a binary one, and both are at 0 V for a binary zero. Since current is running in both directions through the twisted pair the resulting electromagnetic field generated is effectively zero, reducing crosstalk with other communications lines. One set of 4 wires is utilized for the transaction with a twisted pair used for transmission and another pair used for receiving, with each pair having a positive and negative wire. The remaining four wires are used for the "strobe signal" which reads high when the state of the transaction line changes from high to low or vice versa, with a twisted pair accompanying the transmit lines and a pair accompanying the receive lines. This results in an especially robust physical layer which is quite resistant to EMI (electromagnetic interference) from the other communication lines, power lines, and RF signals. A data rate of 25 Mbps is implemented between the bus and CSIE in both directions, allowing images can be transferred to the bus rapidly and fully utilizing the high data capacity of Spacewire. At this rate the CSIE can fill the entire 3.25 GB BCT bus general memory (used for image data) from a science campaign in as little as 18 minutes, reducing the risk of losing data from a power interruption. This interface will send thumbnails, 2x2 binned images, and full resolution images as well as receive commands from the bus to initiate observations. The CSIE also has two digital SE signals controlled by the bus. One is used for programming the CSIE boards and the other is a PPS (pulse-per-second signal) which is utilized for precise timing and synching with the bus clock.

The Bus-Prop interface utilizes RS-422 (Recommended Standard 422). RS-422 is another differential signaling protocol, which utilizes a four-wire interface. RS-422 can operate at up to +/- 6V logic levels, but the implementation VISORS operates at +/- 3.3 V. RS-422 is asynchronous and full duplex. The physical layer is identical to the 4 wires utilized for Spacewire transactions (RS-422 does not utilize strobe lines), except for the differing voltage level. So, there are two sets of twisted pairs, one for TX (transmit) and one for RX (receive) As this protocol also utilizes twisted pair differential signaling, it is also quite robust to crosstalk/EMI. The propulsion RS-422 operates at 115.2 kbps, which is significantly slower than the CSIE-bus interface. However, since the propulsion commands and telemetry are orders of magnitude smaller in data volume, this rate is more than sufficient for this application. This interface will send propulsion health data to the bus and receive commands to perform maneuvers (instructions containing a series of valve opening and closing with accompanying timing data).

The Bus-XLINK interface employs SPI (Serial Peripheral Interface), which is a synchronous, full-duplex interface, utilizing a clock line for timing. The physical layer of SPI is 4 wires: clock, chip select (pulled low during a transaction), MOSI (Master Out Slave In, contemporarily named Serial Data Out, or SDO) and MISO (Master In Slave Out, now called Serial Data In, or SDI). This interface is less resistant to crosstalk and is expected to drop a larger frequency of packets than the differential signal interfaces. It is commonly used for short cable run communications. The advantage of this interface is the high data rate cap as the XLINK system can communicate with the bus at 2 Mbps (clock rate of 2MHz). The XLINK system will receive commands to initiate a link with the other spacecraft, as well as GNC data from the HSA to send over the ISL to the other spacecraft. The XLINK system will forward received GNC data from the other spacecraft back to the HSA as well. There exists the potential to send image data from the DSC to the OSC to relieve the data volume on the DSC or to increase

downlink potential, but this has yet to be defined in the ConOps.

The Bus-PAIB interface is also RS-422. It is identical to Bus-Prop communication line (3.3V, 2 sets of twisted pairs, full duplex). It also operates at 115.2 kbps TX and RX. A line driver is required for this interface as well as the PAIB-CSIE interface to convert the UART (Universal Asynchronous Receiver Transmitter) from the PAIB processor to RS-422. This serial comms line is used by the CSM on the HSA to command subsystem load switches on or off, as well as for sending PAIB, and CVB or LRF (depending on spacecraft) telemetry to the bus for processing or to be downlinked to the ground.

The PAIB-CSIE interface is RS-422 as well. Once again it is identical to the Bus-Prop and Bus-CSIE interface. The baseline implementation employs a data rate of 921.6 kbps. This allows for all images (full resolution, 2x2 binned, and thumbnails) be backed up to the PAIB per the mission ConOps. No hardware flow control is implemented by the CSIE.

The PAIB-CVB interface is I2C (Inter-Integrated Circuit) which is a synchronous, half-duplex data interface. I2C is also known as TWI (Two-wire interface) with one signal SCL (serial clock) used for timing and SDA (serial data) for transmitting data. The shared data line for TX and RX dictates the half-duplex qualities, and lack of chip select means the software layer must include device address wrapping. The CVB shares the I2C line with the PAIB's onboard external ADC. Similar to SPI, this type of interface is more susceptible to EMI and crosstalk, however this is partially mitigated with the slow data rate planned across this interface of 100 kHz. This interface will only send pressure data from the PT mounted within the detector chamber at regular intervals during Early Ops.

The PAIB-LRF interface utilizes LVTTL as the communications line operates at 3.3V logic levels. LVTTL is asynchronous and a full duplex data interface utilizing two wires, with RX and TX lines. Similar to the synchronous communications lines, LVTTL is more susceptible to EMI than the differential signaling approach, but once again this is acceptable as the LRF is not a mission critical component. This data line operates at 19.2 kbps and receives commands to begin the ranging operation as well as returns range telemetry.

Finally, the PAIB-XLINK interface is made up of 22 digital SE signals which the XLINK SDR uses to control the various amplifiers and switches on the XLINK Amplifier and Switching boards. The PAIB simply routes the SDR mezzanine connections to the amplifier board mezzanine connector (which also supplies the amplifiers with the power required to perform their function).

For more detailed information pertaining to the PAIB electrical and data interfaces the reader should refer to the current revision of the PAIB ICD (which is an internal VISORS mission document).

Software Functionality

The PAIB software is the least mature aspect of its design, as priority was placed on defining the interfaces of the subsystem first. As the interfaces evolved, the functional requirements and capabilities of the software have also changed. Given the functional requirements as detailed above and in the RVCM, the commands and telemetry in Table 6 and Table 7 should be addressed in the software.

Table 6: Minimum PAIB Commands

Name	Description
LD_STATE_CMD	Commands the state of all payload load switches
IM_TRANS_CMD	Commands the transfer of a specific image to the BCT Bus
LRF_PWR_CMD	Turns LRF on or off at subsystem level
LRF_MODE_CMD	Changes LRF mode (automatic, slow, fast)
CVB_MDRM_CMD	Commands CVB valve to actuate
PAIB_RST_CMD	Resets the PAIB

Table 7: Minimum PAIB Telemetry

Name	Description
LD_STATE	Returns state of all payload load switches
LD_CURRENT	Returns current of all payload subsystems
LRF_RANGE	Returns range measurements from one science observation
LRF_STAT	Returns the status of the LRF
LRF_ERR_CNT	Returns number of LRF errors sent to PAIB
LRF_ERR_LAST	Returns the last LRF error sent to PAIB
CVB_PRESS	Returns the current pressure of the Mindrum valve
CVB_MDRM_STATE	Returns the state of the valve (open/closed)
PAIB_ERR_CNT	Returns the number of errors on the PAIB
PAIB_ERR_LAST	Returns the last PAIB error
PAIB_RST_CNT	Returns the number of PAIB power cycles

These lists will change as the software matures, but they provide context to what types of commands and telemetry fields should be considered in the FSW development.

PAIB COMPONENT SELECTION

The "Careful COTS" Approach [11]

This strategy for CubeSat avionics design is detailed in a 2013 paper by Sinclair and Dyer which addresses the primary way in which commercial electronics fail in the space environment. This is due to two types of radiation effects: TID (Total Ionizing Dose) which is cumulative damage caused over the mission lifetime by ionizing radiation and SEE's (Single Event Effects) of which there are several flavors, but they are all caused by a single high energy ionizing particle strike. They suggest commercial grade electronics can often be sufficient for the space environment depending on their architecture as well as the radiation severity. Specific lessons learned from their publication are described below and inform the component selection detailed in the following sections. It is recommended the reader review this publication prior to designing CubeSat circuitry.

Key Design Considerations:

1. Radiation Hardened components should be used where possible, especially for mission critical components. Ultimately the nature of CubeSats means limited budgets heavily restrict the ability to utilize rad hardened parts so they should only be used where absolutely critical.

2. Parts without semiconductors (resistors, capacitors etc.), single junction diodes, and BJT's (bipolar junction transistors) can be assumed to be tolerant up to at least 30 krad when properly derated and need only be screened for industrial level workmanship (as opposed to for radiation tolerance).

3. Avoid MOSFET's where possible (note they are often required for power circuitry where voltage drop over a BJT is unacceptable), utilize P-Channel instead of N-Channel MOSFETS, use MOSFETS with minimum gate voltage lower than applied drain voltage, and derate voltage level specifications by 20%.

4. All power circuits should have current and thermal limiting to prevent burnout from SEE's.

5. Use as few parts as possible to reduce the complexity of the design and improve reliability. Complex circuit protections schemes can cause more harm than good in some cases.

Detailed analysis should be conducted but the TID environment experienced over the lifetime of the VISORS mission is forecasted to be less than 10 krads. While there are some voids in the aluminum structure, the chassis of the two spacecraft will block most non-energetic particles and significantly reduce the TID experienced by the avionics within the bus. It is also worth noting that since VISORS is launching during solar maximum to facilitate its science objectives, larger quantities of solar protons are expected whereas GCR (galactic cosmic radiation) will be present in less aggressive concentrations.

Central Processing Unit

The central processing unit selected for the PAIB is the ATmegaS128 MCU (MicroController Unit) [12]. This is a radiation tolerant processor manufactured by Microchip which has an operating range from -55 to 125 C and is rated for TID up to 30 krad with no SEL (Single Event Latchup) below a LET (Linear Energy Transfer) of 62.5 MeVcm^2/mg at the maximum operating temperature. This processor is chosen as GT has experience integrating it with FPrime, a NASA JPL developed CubeSat development framework, on other missions. The processor also has extremely low power draw, all required interfaces to achieve the functions required of the PAIB, and extensive support through the Arduino community [13].

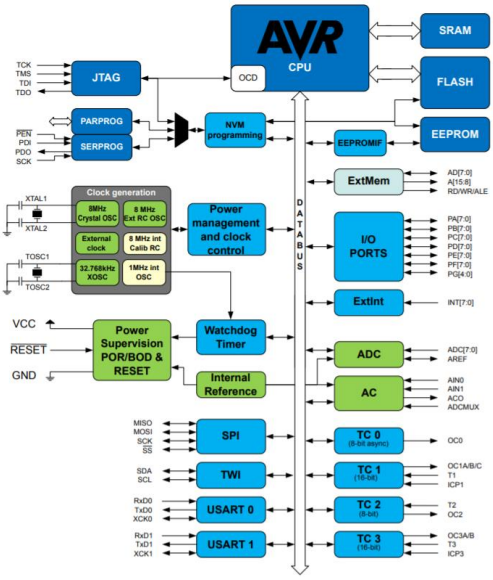

Figure 17: ATmegaS128 Example Diagram [12]

Load Switches

The baseline load switches chosen are Fairchild FPF2700 Adjustable Overcurrent Load Switches [14]. These switches accept all the voltage levels utilized by the payload subsystems (2.8 – 36 V acceptable) and have configurable overcurrent protection between 0.4 A to 2 A. They also provide thermal shutdown protection if the IC reaches temperatures over 140 C. The switches also have a control signal allowing for them to be manually controlled by the MCU. These switches have flight heritage onboard the MicroMAS CubeSat mission. It is important to note that these switches do implement an internal N-Channel MOSFET for power switching and are currently unavailable due to semiconductor shortages. As such it is recommended to investigate alternative load switches prior to proceeding with the design. As mentioned previously, these load switches are used to control power to the subsystems. Two additional load switches are implemented on each PAIB for the power interface to the flash memory, to protect it against overcurrent events during operation and to allow for the flash to be powered off when not being utilized.

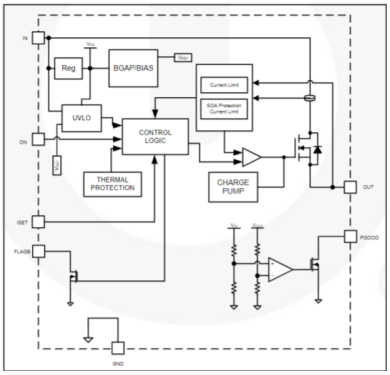

Figure 18: Load Switch Functional Diagram [14]

Current Sensing Amplifiers

The chosen current sensing amplifiers are MAX4071 Bidirectional, High-Side, Current Sense Amplifiers with Reference [15]. This is the next revision of the obsolete MAX471 which has flight heritage on CubeSat by the Sensat Group. The internal reference voltage onboard the IC is preferred as it eliminates the need for an external linear voltage regulator. The amplifiers can operate on supply voltage of 2.7 V to 24 V and has a low supply current requirement of 100 uA. An external sensing/shunt resistor is chosen for each power interface depending on current requirements. These amplifiers can provide output voltages corresponding to the current through the shunt resistor from 0 V to the supply voltage with error less than 1.5%. Recommended shunt resistor sizing details are shown in Table 8.

Table 8: Current Sense Shunt Resistor Sizing [15]

FULL-SCALE CURRENT (A)	CURRENT-SENSE RESISTOR (mΩ)	GAIN (V/V)	V_{SENSE} (mV)	FULL-SCALE OUTPUT VOLTAGE WITH RESPECT TO REF (V)
0.075	1000	50	75	3.75
0.05		100	50	5.0
0.75	100	50	75	3.75
0.5		100	50	5.0
3.75	20	50	75	3.75
2.5		100	50	5.0
7.5	10	50	75	3.75
5.0		100	50	5.0
15.0	5	50	75	3.75
10.0		100	50	5.0

Because there are not enough available ADC pins on the ATmegaS128, an external ADC is required to interface with all the amplifiers. There are other current monitoring IC options (such as the PAC1934 flying on the GT-X series of missions [16]) which boast multiple channels for current sensing on a single IC and utilize I2C to transmit the measured current. These solutions eliminate the need for the external ADC and require fewer parts, but none have been found with flight heritage.

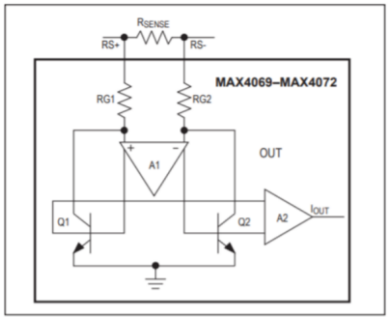

Figure 19: Current Sensing Functional Diagram [15]

External Analog to Digital Converter

The external ADC is a the AD7998 12-bit ADC from Analog Devices operating with a 2.7 – 5.5 V supply [17]. It provides eight input channels, so a single IC is sufficient for all current sense amplifiers used. The ADC has a 2 us conversion time and draws 1.5 mA peak current during operation. These ADC's are being utilized on the GT-X mission but do not yet have flight heritage.

Serial Line Drivers

The chosen line drivers for the RS-422 interface between the CSIE and PAIB as well as BCT bus and PAIB are SN65HVD33 Full Duplex RS-485 Drivers and Receivers (note that it is also designed to operate with RS-422 networks). These are the same line drivers used on the BCT bus for its RS-422 interfaces and have

substantial flight heritage. The part operates at 3.3 V supply and provides autonomous overcurrent and thermal shutdown. Each IC will draw up to 11 mA when transmitting over RS-422.

External Flash Memory

NAND flash is chosen over NOR flash for this non-volatile memory application due to much faster write times and much higher storage density, around one order of magnitude for each. There are three major types of NAND flash memory architecture [18]:

1. SLC (Single-Layer Cell) flash which utilizes one bit per cell of memory. This type has the highest reliability and most read/write cycles (around 100k) but also comes with the highest cost per bit.

2. MLC (Multi-Layer Cell) flash supports two bits per cell of memory. This technology is more affordable than SLC but trades off reliability and read/write cycles down to around 10k cycles.

3. TLC (Triple-Layer Cell) flash is by far the most affordable per bit. It supports 3 bits per cell of memory but is also the least reliable with only around 3,000 read/write cycles.

To mitigate some of these tradeoffs, the PAIB utilizes a pSLC (pseudo-Single-Layer Cell) flash which is MLC flash operating in a mode where only 1 bit is written per cell. This approach allows for the flash to be produced for a lower cost and allows for a higher density storage than traditional SLC, and while not as reliable as SLC, it is more reliable than MLC.

After the flash architecture is selected the flash implementation must be determined. The following three options were investigated:

1. Radiation Tolerant Flash memory utilizing raw flash. This option is two orders of magnitude higher in cost than the other options below but provides the best reliability. It should also be noted that redundant storage would not be required if this option was chosen. This solution is the most robust to radiation and has flown on interplanetary missions. The interface is complex with 80+ pins, and only capacities up to 16 GB are available meaning multiple IC's are required. The cost and complex implementation are reasons why this option was ruled out.

2. SD (Secure Digital) cards are an option that include a built-in controller to aid in reading and writing from the card [19]. This results in a significantly simpler interface and higher density options (32 GB, 64 GB, and 128 GB). Radiation tolerant SD cards are all but obsolete in favor of other memory options, but industrial SD cards are available. However, the controller in the SD card proves to be more problematic than helpful in the space environment as a bit flip in the controller MCU will often result in the controller corrupting and the entire memory being lost. This is due to the implementation of the firmware on the SD card. While not all SD cards have this issue, the firmware can vary between companies or even lot numbers of SD cards, so radiation testing would be required on additional SD cards from a certain lot if this approach is chosen [20]. Power cycling of SD cards during write can also damage the cards. Several CubeSat missions have failed in the past due to corrupted SD cards, so they are typically avoided.

3. eMMC (embedded Multi-Media Card) is another implementation of flash with a built-in controller to simplify the interface down to 4 - 11 pins depending on the mode of operation. These are not plagued by the same issues as SD cards due to a higher reliability firmware and hardware architecture and employs wear-leveling technology to increase the lifetime of the flash. eMMC's also have built-in protection if power is lost during read or write to protect the memory from damage. The main drawback of eMMC is the need to solder it directly to a PCB, and the radiation tolerance specification of eMMC's are not readily available. eMMC's have flight heritage on a few CubeSat missions including PolarLight [21] which has been successfully operating for over 2.5 years (as of April 2021). Proton beam testing (80 MeV) has been performed on eMMC's for robustness to SEE's with no events detected for over 132 equivalent days on the moon [22].

The external flash memory onboard the PAIB used to storage image data for the entire VISORS mission is achieved with two 32 GB SwissBit eMMC's [23]. One eMMC will store the data while the second will serve as a redundant backup. The eMMC's require a 2.7-3.6 V supply and draw 37 mA during read and 83 mA during write each. These flash IC's are not radiation tolerant, but are industrially rated. Nickel plated Brass shields

are installed over the eMMC IC's to provide additional protection from radiation. These eMMC's do not have flight heritage on other missions and exact implementation with the ATmegaS128 must be resolved (choosing to operate in 1-bit, 4-bit, or 8-bit mode). The current implementation utilizes the SPI line and operates the eMMC in 1-bit mode, which somewhat limits the read/write speeds. This interface approach will need to be rigorously tested to determine robustness.

Figure 20: eMMC IC [23] and Copper Shielding

Connectors

Three types of connectors are utilized for all the interfaces on the PAIB. They are chosen since they operate within the industrial temperature range (-40 C to 85 C) and have gold or nickel-plated conductors to avoid tin whiskering. Finally, all insulative materials used to isolate pins from one another are low outgassing, with a TML (total mass loss) of less than 1% and CVCM (Collected Volatile Condensable Material) less than 0.1%. Only the D-sub connectors have flight heritage, but the mezzanine connectors are industrial parts and will be staked to the PCB for increased rigidity.

1. Four Amphenol Bergstak connectors allow the XLINK SDR to interface with the PAIB. These mezzanine (board-to-board) connectors have gold and nickel contacts and an LCP (liquid crystal polymer) insulator. Secondary retention is provided with the standoff used for mounting the PCB's.

2. A DF-12 mezzanine connector is utilized to transmit power and signals routed through the PAIB from the SDR to the amplifier board. This connector type is selected primarily as its mated height matches that of the SDR Amphenol connectors. The contact is gold plated copper with a polyamide insulator. As with the Amphenol connectors board standoffs provide secondary retention.

3. The connectors for all the remaining payload subsystems as well as the BCT bus utilize a combination of Micro and Nano D-Subminiature connectors. These connectors are relatively expensive but are incredibly robust and designed specifically for aerospace applications. The contacts are gold plated copper with LCP insulator. The metal housings of these connectors are Nickel plated Aluminum 6061. These connectors include screw holes to allow for additional mounting points to the PCB they are soldered onto to mitigate shock and vibration. Secondary retention is provided with two machine screws and threaded holes on the mating connectors which can also be further reinforced with thread locker.

Table 9: D-Subminiature Connectors

Connector	P/N	Interface
9 pin Micro	A98055-009	PAIB-Bus
31 pin Nano	A28400-031	PAIB-Bus
	A29100-031	PAIB-CSIE
15 pin Nano	A29200-015	PAIB-PROP
		PAIB-LRF/CVB
	A29100-015	PAIB-Bus

*See PAIB ICD for detailed connector pinouts and descriptions.

An additional connector will need to be selected for an EGSE interface (allowing for programming of the processor as well as monitoring the various serial lines and load switch statuses).

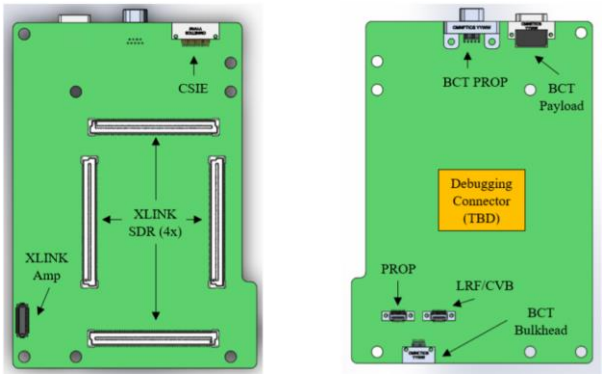

Figure 21: PAIB Connector Locations

Oscillators

The ATmegaS128 can support two external crystal oscillators to serve as clocks in addition to its internal RC (Resistor-Capacitor) oscillator. The first is the datasheet recommended low frequency 32.768 kHz crystal as the processor RTC (Real Time Clock) is optimized for this frequency. As such the remaining crystal selected is 7.3728 MHz as this has zero clock error for driving the 115.2 kbps and 921.6 kbps RS-422 serial interfaces. This crystal can also match the 19.2 kbps LRF data rate with the same 0% clock mismatch.

OPEN RISKS

1. *Component Area Study:* Although the board footprint, mechanical interfaces, and connector locations have been baselined, there has yet to be an area study conducted for all the components required on the PAIB. As such it is uncertain if there is enough surface area on the PCB for all the components. There are several levers to turn here, including selecting different/smaller packages for the various IC's, as currently larger and easier to solder SOIC's (small outline IC) have been selected for all components. This PCB will be trace dense, but this can be mitigated by utilizing additional copper layers, which will not change the thickness of the PCB dramatically. In addition, there is some vertical volume allowance in the AVI stack, so there is possibility of adding an additional PCB with a mezzanine connector below the PAIB and raising the entire stack. It is unlikely this will be required, and presents a significant design change, so it should be avoided if at all possible.

2. *CVB/LRF and Prop Harness Interference:* The current implementation of the PAIB in CAD employs vertical connectors for the CVB/LRF and Prop connectors, as it was initially planned to use right angle harnesses for this interface. Since the right-angle harnesses are not a standard part (will have longer lead times and higher costs to acquire), utilizing a straight connector there results in a tight bend radius which violates the bend radius requirement of the harness. This bend is forced by the nearby chassis wall and cannot be avoided without moving the PAIB upwards. Moving the PAIB upwards is an option, as is using the non-standard part, but both have non-trivial effects on the design and development. Prior to proceeding one of these routes, investigation should be done to see if the connectors can be moved to a different location on the PAIB or if right-angle connectors are feasible.

3. *Software Development:* Software development of the PAIB has yet to begin, which was pointed out as a potential risk during the VISORS CDR (Critical Design Review). The functionality of the PAIB software is scoped out, as is the expected telemetry and commands required for the system to fulfill its function. Of particular interest is investigating what is required to allow the PAIB to receive images from the CSIE in CFDP (CCSDS File Delivery Protocol) format, which is a way to save files within the CCSDS (Consultative Committee for Space Data Systems) architecture [24]. CCSDS is used to route and organize payload telemetry across the payload and bus, as well as for uplink and downlink with the ground. In addition, the ATmegaS128 has had issues on other missions supporting a complex FSW architecture alongside the overhead from FPrime. This resulted in lack of sufficient program memory on the MCU. The scope of the software on the ATmegaS128 should be more accurately estimated to determine if this is a risk for the PAIB as well.

4. *Development Schedule:* The schedule for the PAIB is aggressive, requesting for a fully functional EDU board by early March 2022. However, an earlier "interface" version of this board has been requested by BCT (populated with connectors) to aid in the development of their bus EDU prior to delivery which is slated for late January 2022 (although it is likely this will slip into February). It is also important to note that the PAIB is critical for interfacing the various payload EDU's with the bus EDU, and while one-off harnesses can be built to allow testing of subsystems one at a time with the bus EDU, the PAIB will be required to run testing with the fully integrated EDU system. It is also critical to deliver a PAIB EDU to the XLINK team (perhaps with limited functionality) by late March 2022 so the WSU team can test their various PCB's in the loop with the PAIB due to the coupled nature of the boards on the Avionics Stack.

ACTION ITEMS/NEXT STEPS

1. *External Watchdog Design:* Watchdog timers are utilized in many embedded systems and space applications to mitigate the effects of a latchup or a software bug. The timer will count down in parallel with normal operation of the processor and will reset the processor after the timer reaches a known threshold. As long as the software is operating nominally onboard the system, it will reset the timer periodically before it hits the threshold and resets the processor. However, if the software is unable to reach the point where is resets the watchdog due to an anomaly, the processor will reset and ideally resolve this issue. The ATmegaS128 has a built-in short watchdog timer (resets on the order of milliseconds to seconds) which should be utilized on the PAIB. However, an external longer-term watchdog timer (scale of minutes to hours) is good practice to resolve anomalies which might otherwise not be mitigated with the internal watchdog. A trade should be conducted if such a circuit is sufficiently beneficial for the PAIB design and can be implemented after the first iteration of EDU as it is not critical to the baseline functionality. If such a watchdog is deemed as necessary, it should be designed to be especially radiation tolerant and operate nominally closed, so if the watchdog fails it will not drive repeated resets of the MCU. The sister mission to VISORS, SWARM-EX [25] has developed such a watchdog and could be a useful resource to leverage.

2. *Load Switch Confirmation:* As mentioned in the Component Selection section the baseline Fairchild Load Switches are currently backordered due to the semiconductor shortage. These parts may be available at some suppliers and if so, should be acquired rapidly due to their low cost. It is likely that other alternatives will need to be explored, and if so, care should be taken to select a load switch build around a P-Channel MOSFET if possible. It is important to note other parts may also go out of stock requiring alternatives.

3. *eMMC Selection/Interface:* Additional investigation into memory alternatives such as SSD (solid state drive) should be taken into consideration (including consulting with BCT) before proceeding. Should the eMMC be chosen, scoping of interface is required to fully understand the capabilities of the part when driven from the SPI line on the ATmegaS128 and determine what data rates are possible along the serial line. Ultimately this will need to be tested in the loop with the CSIE data line sending images over RS-422 and the latency of the transfer over to the flash quantified. Because of the ability to operate the eMMC in 1-bit, 4-bit or 8-bit mode, it may also be possible to leverage this parallel data transfer architecture to increase the read and write speeds of the eMMC. This may come in later EDU iterations, but the priority should be placed on creating a design which robustly facilitates this image transfer.

4. *Scoping out EGSE:* Some EGSE will be required to interface the Bus EDU to the PAIB as the Bus EDU employs two full sized D-Sub connectors instead of the three-connector interface on the flight units. As such either an adapter harness must be used (which would result in a complex implementation), or the creation of a connector adapter PCB, which changes these D-Sub connectors to their equivalent Nano and Micro connectors with flight pinouts. This should be a straightforward board design and is a good point of entry for a student who is learning how to use PCB design tools. An umbilical will also be required to interface with the PAIB when it is integrated onto the spacecraft. Ultimately the connector selection should be driven by outgassing, tin whiskering, and vibration constraints, but the connector will not be used during flight so there are several connector options available with the required pinout to allow for monitoring of the PAIB signals.

5. *Schematic Design:* Once the selection of the components detailed above is finalized, work can begin on the first EDU revision of the PAIB schematic within a PCB design tool. The architecture design process should begin with the overall architecture as defined in this document. Then a second pass should be conducted to add supporting components (power capacitors, shunt, gate, and pull down/up resistors, etc.). After the first schematic revision is released, a detailed design review should be conducted with reviewers to verify the circuit architecture. Experienced students within the SSDL, full-time research engineers as well as students from YJSP (Yellow Jacket Space Program) can all be leveraged as reviewers who will provide insightful feedback and resolve any issues.

CONCLUSION

The contents of this document along with the PAIB ICD and other design documentation are intended to share the current development state of the PAIB and provide context for the design decisions made thus far in the development. It should be used as a tool for continuing the development of the subsystem in the future and preparing for manufacture. There are many considerations which must be taken into account when designing a PCB for space applications, beyond the ones mentioned here (radiation and outgassing), as well as design strategies to increase reliability and reduce EMI risk of the system. As the shift to detailed schematic and board design commences, these factors will need to be carefully considered in more granular detail and some iteration of the design will likely be required to converge on an effective solution. The SSDL has numerous resources and lessons learned which can assist with the process to drive this system to a state where it is qualified and ready for flight.

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